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Optimization of Etching Recipes for Si Trenches with Self-Aligned Quadruple Patterning Mask by Transfer Learning NAOTO TAKANO, HYAKKA NAKADA, TAKESHI OMORI, Hitachi, Ltd. Research Development Group — As technologies for semiconductor processing advance, the critical dimensions of devices have shrunk. Proficient engineers have optimized etching recipes (control parameters in etchers) to obtain target etching profiles required for state-of-the-art devices by using knowledge gained from etching results in the process development for previous generation devices. However, as the target profiles have become complicated, the number of etching processes to fabricate state-of-the-art devices has increased. Therefore, the shortage of proficient engineers to optimize recipes for such devices is becoming severe. To solve this problem, we utilize transfer learning to automatically predict the optimal recipes for state-of-the-art devices by learning etching data obtained in the process development for previous generation devices. Our transfer learning model was trained on etching data of Si trenches with a width of 750 nm. The model predicted the optimal recipes for etching Si trenches with a width of 12.5 nm with a self-aligned quadruple patterning mask. We found a vertical trench with an aspect ratio of 8 was etched with one-third of the training data in the conventional machine learning-based methods [1,2]. [1] H. Nakada et al., GEC 2017, [2] H. Nakada et al., GEC 2018

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