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Engineering the electronic properties of nanowires for device applications

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Semiconductor nanowires have recently been recognized as a possible add-on technology to silicon CMOS. Successful integration of nanowires may push the miniaturization of components further and could also bring improved, and completely new, device functions to a chip. In particular, nanowires composed of III-V materials are of interest for applications as they benefit from a small and/or direct bandgap. We will present results from electrical measurements on InAs/InP nanowires grown by chemical beam epitaxy. Changes in the precursors fed to the growth chamber can be made to control the electronic properties of the grown material. In this way it is possible to create atomically sharp heterostructure interfaces, as well as to change the carrier concentration along the wire. The latter can be achieved by controlling the carbon incorporation from the In precursor. It will be shown that heterostructure nanowires can be used in memory cells, and also as single-electron transistors for electrostatic read-out of such cells. Finally, we will discuss the design and application of InAs nanowire-based field-effect transistors, where issues related to lateral and vertical processing of nanowires will be addressed.