MAR07-2006-020181

Abstract for an Invited Paper
for the MAR07 Meeting of
the American Physical Society

Large-Scale Molecular and Nanoelectronic Circuits & Associated Opportunities[1]

JIM HEATH, California Institute of Technology

According to the International Technology Roadmap for Semiconductors (ITRS), by year 2020 it is expected that the most closely spaced metallic wires within a DRAM circuit will be patterned at a pitch of about 30 nm, implying that the conductors themselves will be of a width of around 15 nm. However, virtually every aspect of achieving this technology is considered to be 'red,' meaning that there is no known solution. Nevertheless, ultra-high density (semiconductor and metallic) nanowire circuitry, fabricated at 2020 dimensions and beyond, would be expected to provide a host of value traditional (logic & memory) and nontraditional (sensing, thermoelectrics, etc.) functions. In this talk we will discuss the fabrication and testing of large scale circuitry ($> 10^5$ devices) aimed a these various applications. This will include a 160,000 bit memory circuit that is no larger than a white blood cell, high-performance, ultra-dense & energy efficient logic circuitry, nanowire sensing arrays, and high-performance silicon-based thermoelectric devices. We will also discuss how these circuits may be fabricated on a host of substrates, including plastic.

[1]In collaboration with Elizabeth W. Gilloon, Dunwei Wang, Bonnie Sheriff, Akram Boukai, Yuri Bunimovich, Michael McAlpine, and Young Shik Shin, California Institute of Technology, Department of Chemistry.