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Nanowire Impact Ionization FETs

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One limiting factor in the scaling of transistor technology is the room temperature limit of 60 mV/decade of the inverse sub-threshold slope. As supply- and threshold voltages are scaled down leakage currents rise exponentially causing the standby power of highly integrated circuits to suffer. New types of devices based on band-to-band tunneling [1] or impact ionization [2] have recently been demonstrated that can circumvent the 60 mV/decade limit thereby offering lower leakage currents. We have demonstrated vertical integration [3] of a single surround-gated silicon nanowire field-effect transistor (NW FET) having an inverse sub-threshold slope as low as 6 mV/decade at room temperature that spans four orders of magnitude in current [4]. The transistor shows slopes below 60 mV/decade for supply voltages above 2 V. Due to the use of a top Schottky contact and two ungated regions the devices show ambipolar characteristics with impact ionization for both electron and hole branch. The rather small voltages reduce hot carrier injection into the gate dielectric making threshold voltage shifts and degradation of the performance minimal.

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