

Abstract Submitted  
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**UHV Growth of Graphene on SiC**<sup>1</sup> PAUL CAMPBELL, GLENN JERNIGAN, KEITH PERKINS, BRENDA VANMIL<sup>2</sup>, RACHEL MYERS-WARD<sup>3</sup>, KURT GASKILL, JAMES CULBERTSON, JEREMY ROBINSON<sup>4</sup>, ERIC SNOW, Naval Research Laboratory — We report graphene growth on Si- and C-face semi-insulating 6H SiC in UHV by thermal Si desorption /reconstruction of the remaining C. The SiC was etched in H<sub>2</sub> up to 1580 °C to smooth the surface. XPS shows the H<sub>2</sub>-etched surfaces are covered by an oxide which desorbs at 1000 °C, resulting in a surface containing excess Si. At 1300 °C, the surface becomes stoichiometric in Si and C and a  $\sqrt{3} \times \sqrt{3}$  R30 LEED pattern is observed. At 1350 °C, we observe a  $6\sqrt{3} \times 6\sqrt{3}$  R30 LEED pattern develop when graphene has formed, and a 1x1 LEED pattern for graphite films formed at temperatures greater than 1400 °C. Graphene layers were grown under a variety of temperatures and conditions and characterized using XPS, LEED, AFM, Raman spectroscopy, and Hall effect. Top-gated FETs were fabricated with a wide range of gate lengths (1-25 microns) and gate widths (2-130 microns), and transistor operation was obtained for both single and multiple graphene layers.

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