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Substrate orientation dependence of valley-splitting in Silicon nanostructures NEERAV KHARCHE, SEONGMIN KIM, School of Electrical and Computer Engineering, Network for Computational Nanotechnology, Purdue University, TIMOTHY BOYKIN, Department of Electrical and Computer Engineering, University of Alabama in Huntsville, GERHARD KLIMECK, School of Electrical and Computer Engineering, Network for Computational Nanotechnology, Purdue University — Si nanostructures are being actively perceived for Quantum Computing (QC) devices where valley-splitting (VS) is an important device design parameter. Si is desirable for QC due to its long spin decoherence times, scaling potential and integratability within the present microelectronic infrastructure. Six-fold degenerate valleys in Si interact with each other in the presence of confinements provided by physical dimensions of the nanostructures, and applied electric and magnetic fields. These interactions can result in very-different splittings depending on substrate orientations and inherently present disorders in nanostructures. Surface morphology of Si is highly dependent on substrate orientations and so is the VS. Such surface irregularities are automatically included in supercell tight-binding calculations due to atomistic nature of the Hamiltonian. VS calculations in the Si nanostructures grown on (100), (110), (111) and high index vicinal surfaces will be presented.

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