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CMOS based fabrication of single electron devices on a large scale. VISHVA RAY, RAMKUMAR SUBRAMANIAN, PRADEEP BHADRACHALAM, SEONG JIN KOH, The University of Texas at Arlington — Fabrication of single electron devices requires device components (a Coulomb island, source and drain electrodes) to be arranged with nanoscale precision. This has been so far carried out utilizing techniques such as e-beam lithography, shadow evaporation, electromigration, and scanning probe microscopy, which are not suitable for large-scale fabrication for practical use. Here we present new single electron device architecture and its large-scale fabrication within the framework of CMOS fabrication technology. This has been done by employing vertical electrode configuration where the source and drain electrode separation is controlled with nanoscale precision over an entire wafer. Colloidal Au nanoparticles of 10-20 nm diameter were used as Coulomb islands positioned between the source and drain electrodes. We observed clear Coulomb blockade and Coulomb staircase at room temperature for 10 nm Au nanoparticles with charging energies of $\sim$50 meV, in good agreement with self-capacitance values of 10 nm Au particle. The experimental I-V characteristics also agree well with simulated I-Vs carried out using the orthodox theory.

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