

Abstract Submitted  
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**Stress-driven self-assembly of Si-based nanomembranes for on-chip applications** FRANCESCA CAVALLO, Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden, Helmholtzstrasse 20, 01067-Dresden, Germany, RUDEESAN SONGMUANG, YONGFENG MEI, ARMANDO RASTELLI, OLIVER SCHMIDT, Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden, Helmholtzstrasse 20, 01067-Dresden, Germany — A new field of Si technology based on transferable and engineered nanomembranes has developed with the realization of the fact that properties of bulk Si are preserved in nm-thin layers released from the substrate surface. We demonstrate the ability to pattern Si-based films with nano- scale features, and fold them into a predetermined 3D configuration by finely tuning the strain distribution in the membranes by well-established deposition processes, i.e., MBE, PVD, and thermal oxidation. Our major contributions are the fabrication of integrated microtube resistors based on Si:B/SiGe:B tubes; the use of the Ge condensation technique to tailor the strain distribution in SiGe films on insulator; the manufacturing of fully scalable and CMOS compatible all- semiconductor and hybrid tubes; the fabrication of linear and circular networks formed by interconnected wrinkled structures; the experimental demonstration of light emission from Ge and Si nanoparticles integrated in a tube wall; the observation and investigation of the waveguiding effect along the axis of SiO<sub>x</sub>/Si tubes.

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