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Empirical Pseudopotential Approach to Semiclassical and Quantum Electronic Transport in Nanometer-scale Structures

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The study of electronic transport in semiconductor structures requires an accurate knowledge of the kinematics (*i.e.*, band structure) and of the dynamics (*i.e.*, transport equations and collision processes). As the VLSI technology looks at various sub-10 nm structures as alternatives to the traditional Si CMOS, neither the conventional bulk band structure of the semiconductor nor the semiclassical (Boltzmann) transport equations can be used with confidence to treat the kinematics and dynamics of electronic transport, the former because of size-dependent (quantum confinement) and interface/surface dependent band structure effects; the latter because of the possibility of quantum interference effects at this length scale. Here we will show that empirical pseudopotentials – obtained from the literature and adjusted to yield correct workfunctions, band-alignment, and strain effects – can be used to obtain a sufficiently accurate (as compared to first-principle results) band structure of several systems of technological interest (*e.g.*, thin Si and Ge layers, III-V hetero-layers, nanowires, graphene nanoribbons and C nanotubes). Using this information, semiclassical transport is studied using a Monte Carlo technique and calculating the scattering rates consistently with the band structure information. In some cases, such as in considering scattering with interface and line-edge roughness, the pseudopotential themselves can be used to obtain accurate scattering potentials. The case of high-field transport in Si inversion layers is discussed, showing how the band-structure near the X symmetry point induces a lower saturated electron velocity. Finally, we discuss the wave equation and open boundary conditions which must be employed to handle ballistic quantum transport accounting for the full band structure. Dissipative transport is discussed in the context of a Master equation approach, illustrating this approach with examples ranging from double-gate FETs to Si nanowires.