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Realization of Negative Capacitance with Topological Insulator Based MOS Capacitor[1] HUI YUAN, GMU, KAI ZHANG, ODU, HAO ZHU, HAITAO LI, DIMITRIS IOANNOU, GMU, HELMUT BAUMGART, ODU, CURT RICHTER, NIST, QILIANG LI, GMU, ECE, GEORGE MASON UNIVERSITY TEAM, SEMICONDUCTOR AND DIMENSIONAL METROLOGY DIVISION OF NIST TEAM, ECE, OLD DOMINION UNIVERSITY TEAM — Negative capacitance is one of way to achieve steep subthreshold slope exceeding its thermal limit in metal-oxide-semiconductor field effect transistor (MOSFET). The common materials under study for negative capacitance are ferroelectric thin films. However, the integration of regular ferroelectric materials (e.g., PZT) into semiconductor based devices is usually difficult due to the high temperature required for crystallization and precise control of oxygen percentage in ferroelectric materials. In this work, we found that negative capacitance can be achieved by introducing a topological insulator interlayer into a conventional MOS capacitor. Three-dimensional topological insulators inherently contain a insulator/semiconductor bulk and a gapless conducting surface. When an electric field is added to topological insulator interlayer, imbalanced charge carriers (electrons and holes) would be generated and then accumulate on either surface of the film, resulting in a temporary residual polarization. As a result, a ferroelectric-like hysteresis and negative capacitance are achieved. We believe this approach will be very attractive to achieve steep subthreshold using negative capacitance.

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