

Abstract Submitted  
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**Fabrication of sub-20 nm metal lines on Si substrates** YUKTA P. TIMALSINA, ZONGHUAN LU, LIANG CHEN, KIM LEWIS, TOH-MING LU, Center of Integrated Electronics, Rensselaer Polytechnic Institute, Troy, NY 12180, USA — As line width decreases below 15 nm, the diffusion barriers used in copper (Cu) technology in high performance integrated circuits significantly increase the overall resistivity of interconnects. In this work, we argue that the performance of pure W and Mo lines with line widths smaller than 15 nm could be better than that of Cu lines with barriers. We, herein, present a process of creating Cu, W and Mo metal nanolines on Si substrates using the combination of e-beam lithography (SUPRA 55 Scanning electron microscopy), oblique angle deposition, and lift-off techniques. The integrity of the sub-15 nm nanolines, including the line edge roughness, will be quantified. We shall also report our attempts to measure the resistivity of these nanolines using four point probe techniques. The relative contributions of phonon scattering versus surface scattering will be discussed. The effect of line edge roughness to the overall resistivity will also be presented.

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