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Extrinsic and Intrinsic Charge Trapping at the Graphene/Ferroelectric Interface[1] MOHAMMED HUMED YUSUF, BENT NIELSEN, MATTHEW DAWBER, XU DU, Stony Brook University — In previous works on graphene ferroelectric field effect transistors (GFeFETs), the characteristics of the devices were found to be largely affected by "anti-hysteresis" associated with charge trapping instead of ferroelectric domain switching. In this work, with $PbTiO_3/SrTiO_3$ (PTO/STO) superlattices, the effect of surface adsorbates was largely diminished by tuning the transition temperature of superlattices and depositing exfoliated graphene at an elevated temperature. With the removal of such extrinsic charge traps, the impact from the "intrinsic" defects of the ferroelectric substrate was revealed, inducing fast ($\sim$10 μs) charge-trapping and remaining active even at cryogenic temperatures. The defects manifested themselves as unit-cell deep square pits, which were evident from contact-mode Atomic Force Microscopy (AFM) of the interface. An asymmetry in electron and hole trapping was observed. Optimized superlattice growth conditions minimized the surface defects and subdued the charge trapping associated with it. The result was a robust, ramping speed independent, room temperature ferroelectric switching in GFeFETs. With an ideal interface, the work was further extended to study graphene transport across potential barriers/junctions.

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