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Understanding Electroforming and Resistive Switching in Silicon Dioxide Resistive Memory Devices YAO-FENG CHANG, The University of Texas at Austin, BURT FOWLER, PrivaTran, LLC, FEI ZHOU, KWANG-SUB BYUN, JACK LEE, The University of Texas at Austin, THE UNIVERSITY OF TEXAS AT AUSTIN COLLABORATION, PRIVATRAN, LLC COLLABORATION — Electroforming and resistive switching in SiO2 materials are investigated by anneal temperature, etch time and operating ambient. Thermal anneal in reducing ambient lowers electroforming voltage to small than 10 V. Conductive filaments form within 4 nm of sidewall surfaces in devices with an etched SiO2 layer, whereas most filaments are large than 10 nm from the electrode edge. Switching unpassivated devices fails at 1 atm air and pure O2/N2, with recovery of vacuum switching at about 4.6 V after switching attempts in O2/N2 and at about 9.5 V after switching attempts in air. Incorporating a hermetic passivation layer enables switching in 1 atm air. Discussions of defect energetics and electrochemical reactions lead to a localized switching model describing device switching dynamics. Low-frequency noise data are consistent with charge transport through electron-trapping defects. Low-resistance-state current is modeled by hopping conduction at bias small than 1.5 V. A current overshoot phenomenon starting near 1.6 V is modeled as electron tunneling. Results demonstrate that SiO2-based resistive memory (RM) devices provide a good experimental platform to study SiO2 defects.

Yao-Feng Chang
The University of Texas at Austin

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