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Prospects of III-V Tunnel FETs for Logic Applications¹

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In order to continue and maintain the pace of energy efficient transistor scaling, it is imperative to scale the supply voltage of operation concurrently. In this invited paper, we discuss a promising III-V device architecture such as III-V Heterojunction Tunnel FETs that may break the seemingly inflexible energy vs. performance limit of silicon CMOS transistors and provide high performance, low leakage and low operating voltage for future logic transistor technology. Unlike conventional MOS-FETs, the Tunnel FET (TFET) architecture employs a gate modulated Zener tunnel junction at the source which controls the transistor ON and OFF states. This scheme fundamentally eliminates the high-energy tail present in the Fermi–Dirac distribution of the valence band electrons in the p+ source region and allows sub- kT/q steep slope device operation near the OFF state. This allows Tunnel FETs to achieve a much higher ION–IOFF ratio over a small gate voltage swing. A major challenge in the demonstration of high performance Tunnel FET is the limited rate of tunneling across the Zener junction which results in low drive current. Our results show, for the first time, that the on-current bottleneck in Tunnel FETs can be overcome by careful bandgap engineering.

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