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Gate-defined Single Electron Transistor in a Graphene-MoS2 van der Waals Heterostructure KE WANG, Department of Physics, Harvard University, Cambridge, MA 02138, USA, TAKASHI TANIGUCHI, KENJI WATANABE, National Institute for Materials Science, Namiki 1-1, Tsukuba, Ibaraki 305-0044, Japan, PHILIP KIM, Department of Physics, Harvard University, Cambridge, MA 02138, USA — We report experimental demonstration of fabrication of laterally confined single electron transistor (SET) on MoS2 transition metal dichalcogenide (TMDC) semiconductor. A few atomic layers of MoS2 single crystals are encapsulated in hBN layers in order to improve mobility of 2-dimensional (2D) electron channel. Graphene layers are employed to provide Ohmic contact to the TMDC channels. The laterally confined quantum dots are formed by electrostatically depleting the near-by 2D channel employing local gate fabricated by electron lithography. Typical SET transport signatures such as gate-tunable Coulomb blockade have been observed. We have demonstrated the quantum confinement can be sensitively tuned to adjust the dot-reservoir coupling. The work paves way for more complicated device structure such as valley-spin filter and vertically coupled quantum dots in Coulomb drag devices.

Ke Wang
Harvard University

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