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Achieving Thermodynamic Limit of Subthreshold Slope in Nanoscale Schottky Barrier MOSFET with Pillar Structure Inserted[1]

JUNG-YONG LEE, SUNGCHUL JUNG, KIBOG PARK, Ulsan Natl Inst of Sci Tech — As the device size decreases continuously by scaling in the current Si CMOS technology, subthreshold slope which is related to device operation and leakage current becomes more and more important. Especially, the drain induced barrier lowering (DIBL) modulation for improving subthreshold slope in metal/oxide/metal field effect transistor (MOSFET) is difficult to achieve. We propose a new device structure, edge-over Schottky Barrier MOSFET (EO-SB-MOSFET), which shows low DIBL and subthreshold slope approaching the thermodynamic limit of 60 mV/DEC at room temperature. EO-SB-MOSFET has a pillar structure which elongates the transistor channel by forming it over the edge of pillar. Hence, EO-SB-MOSFET has a much longer channel compared with planar MOSFET in the same pitch. We performed 2-dimensional TCAD modeling on an EO-SB-MOSFET with channel lateral size of 6.5 nm and pillar height of 36 nm. The TCAD modeling predicts DIBL of ∼5 mV/V, subthreshold slope of ∼61.3 mV/DEC, and off-state current of ∼0.1 nA/μm at drain bias 0.5 V. It is also noticed that the subthreshold slope gets further close to the thermodynamic limit as the pillar height increases.

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