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Novel Heterostructure Devices for Ultra-Scaled Logic[1]

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Continuing increases in circuit complexity and capability for logic and computational applications as well as for emerging low-power distributed systems require fundamental advances in device technology and scaling. Dimensional scaling of conventional devices are approaching fundamental limitations. In addition, due to power constraints, devices capable of achieving switching slopes (SS) steeper than 60 mV/decade are essential if conventional computational architectures are to continue scaling. Similarly, low power systems such as distributed sensing applications also benefit from devices capable of delivering high performance in low-voltage operation. Tunneling field effect transistors (TFETs) are one promising alternative to achieve these objectives. A great deal of work has been devoted to realizing TFETs in Si, Ge, and narrow-gap III-V materials, but the use of two-dimensional materials and III-N heterostructures offer unique opportunities. From physics-based simulations, GaN/InGaN/GaN heterostructure TFETs offer the potential for achieving switching slopes approaching 20 mV/decade with on-current densities approaching 1 mA/μm in nanowire configurations, while recent results in two-dimensional materials have also shown potential for sub-thermionic switching slopes. In this talk, the operational principles of candidate devices for steep switching will be described, and device design and performance considerations will be discussed. In addition, experimental efforts demonstrating these devices will be reviewed, and the future prospects for these and related devices to enable future generations of scaled technologies will be discussed.

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