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Atomistic Modeling of Interconnect Resistance in Emerging Semiconductor Technologies OSCAR D. RESTREPO, EDUARDO C. SILVA, BYOUNG YOUP KIM, CRAIG CHILD, MURALI KOTA, GlobalFoundries, Malta, NY 12020 USA — With extreme scaling in semiconductor devices, power consumption due to Back-End-Of-Line (BEOL) interconnect resistance is critical in the performance of semiconductor chips. A typical via structure consists of Cu/diffusion barrier/binder/Cu. Besides the intrinsic resistance of the Cu Via, the TaN diffusion barrier, Co binding layer, and defects such as voids contribute to the overall BEOL resistance. To overcome the TaN resistance at the via interface, a method was developed for selective nitridation of via dielectric side walls, avoiding the formation of a TaN layer between the two Cu layers. Here, we perform Ab-initio electronic structure and transport calculations to understand the impact of α and β phases of Ta, as well as replacing Co with Ru. We find excellent agreement with the experimental measurements of 30-40% reduction in resistance for β-Ta compared to TaN, and predict that α-Ta will further reduce the interface resistivity by 15%. We also found that replacing Co with Ru causes an increase in the resistivity, even though void formation is reduced, which agrees with experimental results. This work lays the foundation for future work in optimizing BEOL resistance that is critical to the performance of nano-device based semiconductor chips.

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