

Abstract Submitted
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Silicon transistors in reduced dimensions FELIX SCHUPP, University of Oxford, MUHAMMAD MIRZA, DONALD MACLAREN, University of Glasgow, ANDREW BRIGGS, University of Oxford, DOUGLAS PAUL, University of Glasgow, JAN MOL, University of Oxford — Junction-less nanowire transistors are being investigated for deeply scaled CMOS technology. To date almost all simulations to optimise the technology have been based on 3D or 2D modelling schemes. Here we will present measurements that unambiguously demonstrate 1D transport in sub-10 nm junction-less nanowires. The 1D nature of our device allows for excellent gate modulation despite doping concentrations being well above the metal-insulator transition. We find subthreshold slopes of 66 mV/dec, on- to off-current ratios above 10^8 and on-currents of 1.15 mA/ μm for a gate overdrive of 1.0 V from transistors with a gate-length of 150 nm at room temperature. We observe Universal Conductance Scaling as a function of voltage and temperature similar to previous reports of transport in 1D systems. In low temperature transport experiments Quantum interference effects including signatures of subband filling are observed. We extract a phase coherence length of 15.7 nm from universal conductance fluctuations, suggesting possible ballistic transport in shorter channels. Our experiments demonstrate the importance of dimensionality in ultra-scaled CMOS devices and highlight the need for 1D device modelling schemes.

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