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George E. Pake Prize Lecture: CMOS Technology Roadmap: Is Scaling Ending?

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The development of silicon technology has been based on the principle of physics and driven by the system needs. Traditionally, the system needs have been satisfied by the increase in transistor density and performance, as suggested by Moores Law and guided by "Dennard CMOS scaling theory". As the silicon industry moves towards the 14nm node and beyond, three of the most important challenges facing Moores Law and continued CMOS scaling are the growing standby power dissipation, the increasing variability in device characteristics and the ever increasing manufacturing cost. Actually, the first two factors are the embodiments of CMOS approaching atomistic and quantum-mechanical physics boundaries. Industry directions for addressing these challenges are also developing along three primary approaches: Extending silicon scaling through innovations in materials and device structure, expanding the level of integration through three-dimensional structures comprised of through-silicon-vias holes and chip stacking in order to enhance functionality and parallelism and exploring post-silicon CMOS innovation with new nano-devices based on distinctly different principles of physics, new materials and new processes such as spintronics, carbon nanotubes and nanowires. Hence, the infusion of new materials, innovative integration and novel device structures will continue to extend CMOS technology scaling for at least another decade.