

Abstract Submitted  
for the MAR16 Meeting of  
The American Physical Society

**Effects of Ordered Stacking Faults on Electrical Transport Properties in Silicon Nanowires** MARC COLLETTE, Concordia University, Montreal, OUSSAMA MOUTANABBIR, Ecole Polytechnique, Montreal, ALEXANDRE CHAMPAGNE, Concordia University, Montreal — Lattice defects in silicon nanowires (SiNWs) allow the exploration of the fundamental physics governing transport mechanisms. We study charge transport in SiNW transistors with stacking faults in the 3C sequence, producing local hexagonal ordering. This structure leads to polytype SiNWs with distinct properties for novel applications in thermoelectronics. Since charge carrier and phonon behavior depend on crystal structure, these planar defects affect the transport properties of the nanowire. We grow our SiNWs using a VLS method, with stacking faults induced during growth. Structural characterization of each SiNW is done with Raman spectroscopy to quantify hexagonality. Individual nanowires are located and contacted using different metals to understand the Schottky barrier of the contacts at the SiNWs. We suspend 2  $\mu\text{m}$ -long SiNW devices using a wet oxide etch to uncouple the SiNW from the substrate. We study the electrical properties by  $I$ - $V$  measurements across the FET device while modulating the applied back gate voltage. Our initial data show that the presence of stacking faults causes an increase in resistivity by two orders of magnitude, thus greatly hindering charge transport through the SiNW.

Marc Collette  
Concordia University, Montreal

Date submitted: 06 Nov 2015

Electronic form version 1.4